Yuxuan Jiang

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Education

University of Illinois Urbana-Champaign, Urbana, IL 2019 – Present

B.E. in Computer Engineering, expected 2023

Zhejiang University, Haining, Zhejiang 2019 – Present

B.E. in Electronics and Computer Engineering, expected 2023

Research Experience

Acto: Automatic Testing of Cloud System Operators (In Submission) Feb 2022 – Present

Research Intern Mentored by Prof. Tianyin Xu at UIUC and Prof. Owolabi Legunsen at Cornell University

An automatic bug finding tool for Kubernetes operators. The team is currently working to submit the paper to a top system conference.

- Raised and designed the input exploration strategy to intentionally test the error handling logic of an operator. Designed the oracle to capture unhealthy system states, which reduces false negatives and enriches alarm description.
- Interfaced Kubernetes ApiMachinery to collect system snapshot for oracle and later debugging
- Re-implemented the Acto architecture, enable parallel testing, and support multiple cluster runtime (Kind, K3D, MiniKube, etc.)
- Inspected experiment results; Found 18 (32% of all bugs found by Acto) unknown bugs in 3 popular Kubernetes operators, 14 (50% of all bugs fixed) of them are now fixed; Contributed patches to the bugs
- Designed academic poster and presented the project in an internal event

Slooo: A Fail-slow Fault Injection Testing Framework (In Review) May. 2021 – Feb. 2022

Research Intern (remote) Mentored by Prof. Tianyin Xu at UIUC

A Xonsh-based fault injection framework that can be used for fail-slow fault-tolerance evaluation of distributed systems.

- Implemented features including test-bed provisioning for local machines and cloud providers, role-based fault injection, system usage monitoring and result visualization
- Co-designed the interface of Slooo that reduces developers' effort (e.g. lines of code) to apply Slooo to target systems
- Used Slooo to investigate fail-slow tolerance of Etcd and PolarDB

Cloud Architecture Research Intern – MSR-Asia Oct 2022 – Present

Research Intern Mentored by Dr. Shilin He at Microsoft Research Asia

- Conducting empirical study on configuration-induced failures in container orchestration systems, such as Kubernetes
- Performed an presentation to introduce research works on configuration management issues internally

Publications

- **Slooo: A Fail-slow Fault Injection Testing Framework** (In review since Nov 2022)
  Varshith Bathini, Sachin Ashok, **Yuxuan Jiang**, Shuai Mu, Tianyin Xu

Professional Activities

2021 Internet+ Innovation and Entrepreneurship Competition Aug. 2021

Team Leader

- Led a team of 4 students to compete in the largest business contest for Chinese college students, ranked **top 3 out of 142** in Zhejiang province
- Proposed the idea of "City Brain as Containerized Data Centers (D-HPC)" and conducted business analysis

MusePot: online Beat Trading Platform (student start-up) Jun. 2021 - Jun. 2022

Backend Developer Developed an online music trading app with MERN Stack

TEACHING AND SHARING

Microsoft Learn Student Ambassador Nov. 2021 – present

- Taught basics concepts of linux, git, github, windows subsystem for linux, etc. to chinese and international students. Teaching materials credited to MIT 6.NULL and Microsoft Learn
- Organized events on career planing; arranged workshops to help individual students with specific problems they are facing

Unimate - Teaching and Learning Assistant Oct. 2021 – Jan. 2022

- Mentored international students who cannot come to China due to travel restrictions at Zhejiang University International Business School
- Held weekly TA sessions to help students with their assignments and exams.
- Organized bi-weekly social events to engage remote students and give them a sense of belonging

PROJECTS

Magic Tower FPGA

The FPGA re-implementation of a classic RPG game. Designed tile-based and framebuffer-based graphics system to balance resource usage, performance and image quality; To achieve 60Hz refresh rate, implemented an SRAM controller to simulate dual-port access for a single-port chip; Designed DMA interface to cache resources from SDRAM to onchip memory

Distributed Transaction System

Implemented in Golang; Used Timestamp Ordering Protocol and 2 Phase Commit to ensure ACI(D); gRPC is used for communication between servers and clients

Unix-like Kernel

Implemented a toy kernel on i386 architecture with GDT/IDT Support, Memory Paging, Terminal Driver (VGA Driver under Text Mode), Real-Time Clock Driver and Virtualization, Basic Set of System Calls, Keyboard Driver and Input Buffer, Read-only File System, User-level Code Loader, Round-robin Style Scheduling

CNN Convolution Optimization

Adopt advanced techniques to optimize memory access latency and reduce operational costs. Performance reached the 10th out of 200 students in the ECE408 class at UIUC

HONORS AND AWARDS

Outstanding Undergraduate Student, Zhejiang University 2022, 2021, 2020
Scholarship for Outstanding Students, Zhejiang University 2020
Dean's List, Zhejiang University 2020